Crosstalk in SiC Power MOSFETs for Evaluation of Threshold Voltage Shift Caused by Bias Temperature Instability

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Keywords

«Silicon Carbide (SiC) », «MOSFET», «Reliability», « Wide bandgap devices »

Abstract

Threshold voltage drift from Bias Temperature Instability is known to be a reliability concern for SiC MOSFETs. Negative bias temperature instability (NBTI) results from positive charge trapping at the gate dielectric interface and is more problematic in SiC due to the higher interface trap density. Turning SiC MOSFETs OFF with negative voltages to avoid Miller coupling induced cross-talk can cause V_{TH} shifts in periods with long standby duration and high temperatures. This paper proposes a novel test method for BTI characterization that relies on measuring the shoot-through current and charge during switching transients. The method exploits the Miller coupling between 2 devices in the same phase and uses the shoot-through current from parasitic turn-ON to monitor V_{TH}. Standard techniques require the use of static measurements (typically from a parameter analyzer or a curve tracer) to determine the threshold voltage shift. These conventional methods can underestimate the V_{TH} shift since the recovery from charge de-trapping can mask the true extent of the problem. The proposed methodology uses the actual converter environment to investigate the V_{TH} shift and should therefore be of more interest to applications engineers as opposed to device physicists. Furthermore, it avoids the problem of V_{TH} recovery and is therefore more accurate in V_{TH} shift characterization.

Introduction

The primary advantage of power MOSFETs and IGBTs over contemporary power devices is the presence of an insulated gate that is easy to drive, reliable and has low ON-state power dissipation [1]. The oxidation of silicon to form SiO_2 typically results in low interface, fixed oxide and near-interface trap density. However, in SiC, the presence of carbon atoms that do not readily oxidize at the semiconductor/oxide interface results in increased interface and near-interface traps which degrade the oxide integrity [2]. Furthermore, the reduced band-offsets at the conduction and valence band edges of the SiC/SiO_2 mean less thermal energy is required for thermionic emission across the dielectric [2].

Since the device loses controllability and fails in the event of dielectric degradation, gate oxide reliability is a critical component of overall power device reliability [3, 4]. It has been reported that SiC MOSFETs perform less on time-dependent dielectric breakdown and generally show reduced oxide reliability compared to silicon devices [5]. V_{TH} shift from charge trapping is a critical concern and is usually referred to as Bias Temperature Instability (BTI) [2, 6-9]. Upward V_{TH} shift from positive bias temperature instability (PBTI) can cause marginal increments in the conduction losses while downward

V_{TH} shift from negative bias temperature instability (NBTI) can cause electrothermal failure from over-currents/current crowding due to loss of gate synchronization in parallel devices [10]. Turning SiC MOSFETs OFF with negative voltages to avoid Miller feedback capacitive effects [11] leaves SiC devices vulnerable to NBTI. Hence, assessing BTI induced V_{TH} shifts in SiC MOSFETs has become a main research topic in recent years [2, 6-9, 12, 13].

Investigating the reliability of SiC power MOSFETs usually involves the application of an accelerated stress voltage (that exceeds the rated gate voltage) at a defined temperature, after which static and/or dynamic characteristics are measured to determine the V_{TH} shift. The value of the gate voltage stress, the temperature of the device and the duration of the stress are parameters affecting the magnitude of the threshold voltage shift [7, 14-16]. Regarding V_{TH} measurement for BTI characterization, there are different factors that make the determination of the real V_{TH} shift challenging. First, the measured V_{TH} is affected by factors like the measurement speed, bias interruption and stress reapplication [8, 17]. The gate voltage sweep direction does also affect the measured V_{TH}, defining a phenomenon called threshold voltage hysteresis [2].

The principal issue of BTI stress and characterization in SiC MOSFETs is the recovery of V_{TH} after stress removal [2, 17, 18]. Considering a positive gate voltage, when the stress is removed the traps release electrons whereas in the case of a negative voltage stress, the traps release holes. This process is known as trap relaxation, causing a V_{TH} shift recovery. A gate voltage of the opposite polarity accelerates the recovery of the V_{TH} shift, as different authors have identified [5, 16]. This recovery of V_{TH} may have serious implications for qualification of power devices, as the measured V_{TH} can be not representative of the actual V_{TH} after stress and before recovery [9, 19]. Methods able to capture a more accurate V_{TH} shift have been presented by different authors in [2, 8, 12, 18].

In this paper, a technique that uses the momentary short circuit current that results from Miller coupling between devices on the same phase leg is developed and tested as a technique of monitoring BTI and its implications. By using the peak short circuit current and total short circuit charge, the drift and recovery of V_{TH} can be tracked. Although there is significant research about quantification and evaluation of BTI-induced threshold voltage shifts [2, 8, 12, 18], the investigations on the implications of BTI are scarce in the literature [6, 20-22]. The importance of the results presented in this paper is that they show how the proposed methodology can be used for evaluating the implications of BTI in a converter leg.

Test circuit for evaluation of parasitic turn-ON (cross-talk)

The method for evaluation of BTI is based on the parasitic turn ON or "cross-talk" between devices in a phase leg of a converter. Cross-talk simply refers to the unwanted turn-ON of a power device due to voltage commutation of the complementing device in the phase leg and Miller capacitance coupling [11, 23]. The test circuit for the measurements of BTI induced short circuit current is shown in Fig. 1, together with a picture of the laboratory setup. The circuit is comprised of a half bridge configuration with a load resistance connected in parallel with the bottom side power device.

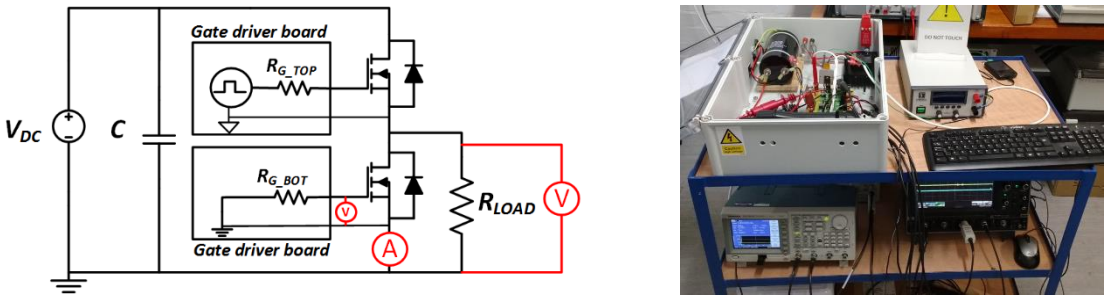

Fig. 1 (a) Schematic test setup for evaluation of BTI using shoot-through currents. A customizable gate driver board is used for both the top and bottom device (b) Laboratory setup

The technique proposed here is based on the fact that the total shoot-through charge depends on the threshold voltage, hence, any change in V_{TH} from BTI can be detected by the total shoot-through charge

in the bottom side device. This technique of monitoring BTI induced V_{TH} shift is more suited to applications engineers that are more interested in the circuit consequences of V_{TH} shift as opposed to the phenomenon itself i.e. it demonstrates the circuit level consequences of the phenomenon under real switching conditions.

There are 3 distinct time phases in the use of this circuit and how it uses the Miller induced capacitive feedback effect to characterize BTI and its impact on circuit operation. The device switched is the top device in Fig. 1, whereas the device subjected to parasitic turn-ON is the bottom device

Phase 1: In the initial state, both devices are OFF. The DC link voltage V_{DC} falls across the top side device because the load resistance is much smaller than the OFF-state impedance of both devices. The gate of the top side device is triggered with a pulse thereby switching the device ON and forcing the DC link voltage V_{DC} on the bottom side device. The rate at which the top side device is switched, which is controlled by the top side gate resistance R_{GTOP}, will determine the drain-source voltage switching rate dV_{DS}/dt across the bottom side device.

Phase 2: As the bottom side device experiences a dV_{DS}/dt across its drain-source (or collector-emitter) terminals, a Miller current flows through the non-linear gate-drain capacitance C_{GD}. The magnitude of this Miller current will be given by the value of the Miller capacitance multiplied by dV_{DS}/dt, as defined in equation (1)

$$I_{Miller}=C_{GD}\cdot dV_{DS}/dt \tag{1}$$

This Miller current flows through the bottom side device gate resistance as well as charges the gate-source capacitance C_{GS} of the bottom side device. This causes a parasitic gate voltage across the gate-source of the bottom side device. The magnitude of this V_{GS} will depend on the Miller current and the bottom side gate resistance R_{G_BOT}. Considering the switching device the top side device in Fig. 1, the parasitic gate-source voltage $V_{GSparasitic}$ resulting from the Miller current can be calculated using equation (2).

$$V_{GSparasitic} = R_{G\_BOT} C_{GD} \frac{dV_{DS}}{dt}\left(1 - e^{-\frac{t}{R_{G\_BOT}(C_{GS}+C_{GD})}}\right) \tag{2}$$

Phase 3: If the parasitic gate voltage of the bottom side device exceeds the threshold voltage of the device, a shoot-through current flows. The peak current and the total duration of the current will depend on the parasitic gate voltage, device transconductance and the threshold voltage. The parasitic gate voltage depends on switching rate of the top side device (determined by R_{GTOP}), the Miller capacitance of the bottom side device and the bottom side gate resistance (R_{G_BOT}), as given by equation (2).

Using the circuit presented in Fig. 1, shoot-through measurements have been made on a 1200 V SiC planar MOSFET from Littelfuse (Fig. 2). The DC link voltage V_{DC} used was 400 V, the load resistance R_{LOAD} 500 Ω and a basic gate driver circuit, based on the gate drive IC HCNW-3120 was used. The gate parasitic gate voltage was measured using a differential probe model TA043 from Pico Technology, the drain-source voltage was measured using a high voltage differential probe GDP-100 from GW Instek and the current was measured using a current probe model TCP312 from Tektronix. The waveforms were captured using an oscilloscope Wavesurfer 104MXs-B from Lecroy. Keeping the gate resistance of the top device fixed and changing the value of R_{G_BOT}, the parasitic turn-ON can be exaggerated and studied easily. The gate driver voltage of the top device is adjusted to the recommended driving voltage of the evaluated SiC MOSFET, whereas the bottom device is held OFF at V_{GS}=0 during the experiments. The measurements were done at ambient temperature and 4 combinations of R_{G_TOP} and R_{G_BOT} were evaluated: R_{G_TOP} = 33 Ω/R_{G_BOT}=10 Ω, R_{G_TOP} = 33 Ω/R_{G_BOT} = 33 Ω, R_{G_TOP} = 33 Ω/R_{G_BOT} = 68 Ω and R_{G_TOP} = 33 Ω/R_{G_BOT} = 220 Ω.
Fig. 2(a) shows the drain-source voltage V_{DS} across the bottom side device as the top side device is gated with a pulse, Fig. 2(b) shows the parasitic V_{GS} voltage on the bottom side device and Fig. 2(c) shows the

measured shoot-through current I_{DS} through the bottom device during switching for a 1200 V SiC planar MOSFET from Littelfuse.

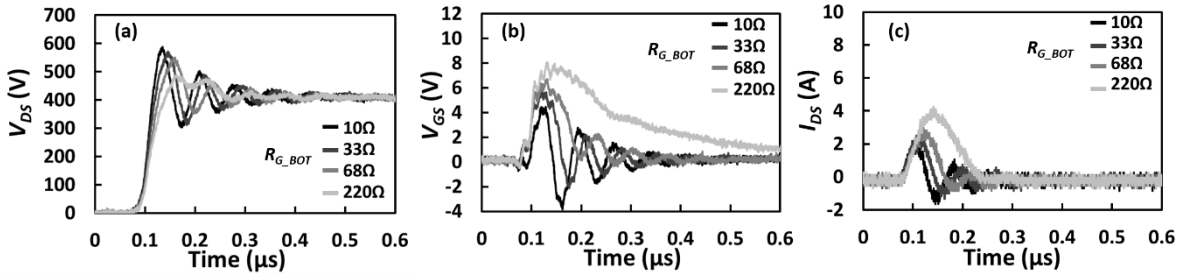

Fig. 2 SiC planar MOSFET Littelfuse (a) Drain-source voltage of bottom side device during cross-talk, (b) Parasitic gate voltage of bottom side device during cross-talk, (c) Shoot-through current of bottom side device during cross-talk

Depending on the device characteristics and its susceptibility to parasitic turn-ON, the presented technique can be more effective. The susceptibility to parasitic turn-ON of a set of SiC MOSFETs has been evaluated as a preliminary step in this study and the results are shown in Fig. 3 to Fig. 5. The devices evaluated are a 1200 V SiC Planar from ST (Fig. 3), a 900 V SiC Planar from Cree/Wolfspeed (Fig. 4) and a 650 V SiC trench MOSFET from Rohm (Fig. 5).

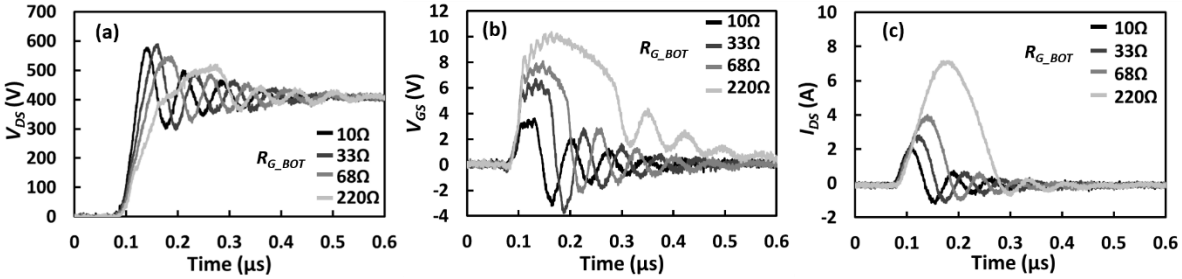

Fig. 3 SiC planar MOSFET - ST. (a) Drain-source voltage of bottom side device during cross-talk, (b) Parasitic gate voltage of bottom side device during cross-talk, (c) Shoot-through current of bottom side device during cross-talk

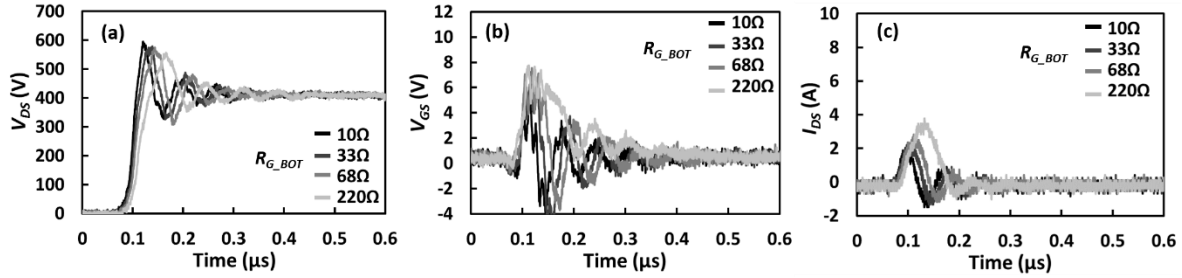

Fig. 4 SiC planar MOSFET - Wolfspeed (a) Drain-source voltage of bottom side device during cross-talk, (b) Parasitic gate voltage of bottom side device during cross-talk, (c) Shoot-through current of bottom side device during cross-talk

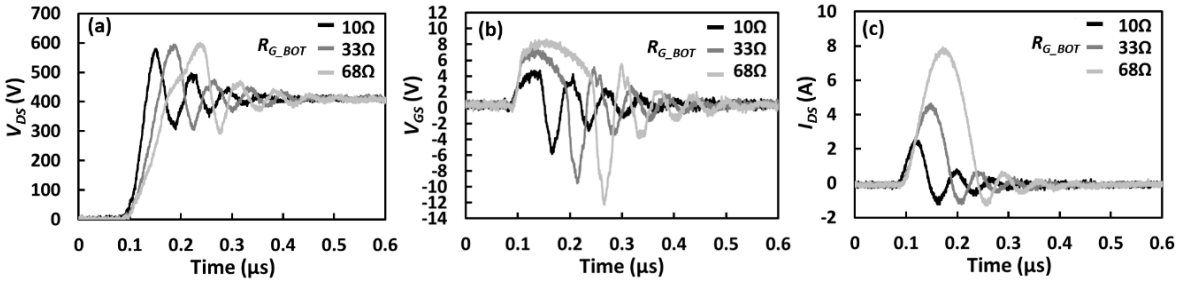

Fig. 5 SiC trench MOSFET - ROHM. (a) Drain-source voltage of bottom side device during cross-talk, (b) Parasitic gate voltage of bottom side device during cross-talk, (c) Shoot-through current of bottom side device during cross-talk

Analyzing Fig. 2 to Fig. 5, it is clear that the 4 evaluated SiC MOSFET have different susceptibility to parasitic turn-ON. In the case of the SiC planar MOSFET from Cree/Wolfspeed, even for a worst case

of R_{G_BOT}=220 Ω, the device is not significantly affected by parasitic turn-ON (less than 4 A peak). The planar MOSFET from Littelfuse is similarly affected by parasitic turn-ON, with a peak current of around 4 A. The device from ST shows good immunity to parasitic turn-ON until the bottom gate resistance is increases over 68 Ω, with a peak shoot-through current of around 7 A for R_{G_BOT}=220 Ω. The trench MOSFET from Rohm is the device which is more affected by parasitic turn-ON, with a peak shoot-trough current of 8 A for a bottom gate resistance R_{G_BOT}=68 Ω. In the circuit used for these tests, the parasitic gate voltage of the SiC trench MOSFET exhibits a characteristic negative spike, which may have a negative impact on the reliability of the gate oxide. This indicates that additional circuitry may be required for improving the transient behavior of the parasitic gate voltage.

In the next section it will be shown how the shoot-through current caused by cross-talk can be used for monitoring BTI-induced V_{TH} shifts.

Evaluation of threshold voltage shifts using cross-talk

Accelerated stress tests and impact on shoot-through current

In order to study the impact of a change of V_{TH} in the measured shoot-through current, accelerated high temperature gate bias stress tests have been performed on the SiC power MOSFETs. For these tests gate voltages higher than the nominal value were applied to the gate terminal at a temperature of 150 °C for one hour. After the stress, the gate and source terminals were shorted (V_{GS}=0) and the device was left to relax at ambient temperature for a minimum time of 1 hour. This allows to assume a more permanent shift of V_{TH} before characterization. The stress voltage is a negative voltage, hence, a downward shift in V_{TH} is expected. This downward shift will translate into an increase of the parasitic shoot-through current. An example of these type of accelerated stress tests for evaluating the impact of the change of V_{TH} in the transfer, output and dynamic characteristics were performed in [12, 21, 24].

It is important to mention that the main objective of these tests is to obtain a device with a modified V_{TH} to evaluate its impact on the shoot-through current. The aim of the investigations in this paper is developing a testing methodology rather than evaluating the reliability of the gate oxide and different stress voltages were used depending on the device evaluated, to obtain a more permanent shift of the threshold voltage [12, 21, 24].

As demonstrated in the previous section, the selection of the gate resistances is fundamental for the effectiveness of this method. A 1200 V planar SiC MOSFET from Littelfuse was subjected to subjected to 1 hour stress at V_{GS}=-36 V and 150 °C. The post-stress characterization was done after 1 hour relaxation at V_{GS}=0. The unstressed and stressed shoot-through characteristics were obtained at ambient temperature, using the test setup shown in Fig. 1, and the results are shown in Fig. 6.

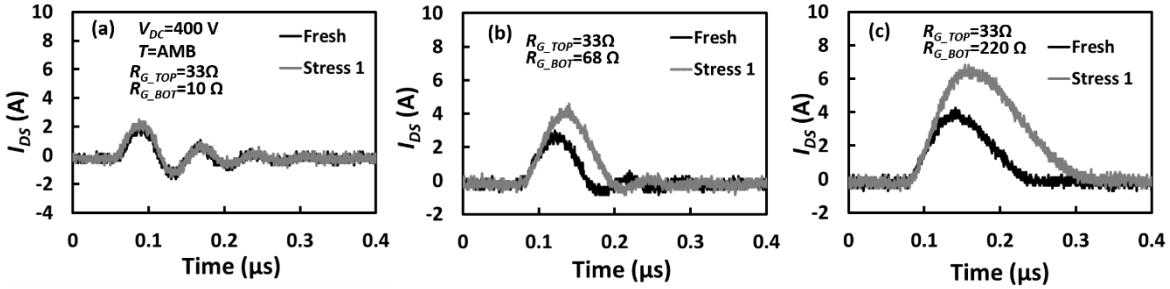

Fig. 6 SiC planar MOSFET from Littelfuse. Unstressed and NBTI stress. Impact of the gate resistance combination on the measured shoot-through current. (a) R_{GTOP}/R_{GBOT} of 33 Ω/10 Ω, (b) R_{GTOP}/R_{GBOT} of 33 Ω/68 Ω, (c) R_{GTOP}/R_{GBOT} of 33 Ω/220 Ω

Fig. 6 shows the shoot-through currents measured using a different set of gate resistance combinations pre-stress and after NBTI stress. Since the stress voltage was negative, a downward shift in V_{TH} results in a higher peak shoot-through current and a larger shoot-through charge. The results in Fig. 6 highlight

the importance of the selected resistors for the effectiveness of the proposed method. Using a gate resistance combination of R_{G_TOP}/R_{G_BOT} = 33 Ω/10 Ω minimizes the impact of parasitic turn-ON, thereby the measured shoot-through currents show no impact of the V_{TH} shift caused by BTI. However, using the gate resistance combinations of R_{G_TOP}/R_{G_BOT} = 33 Ω/68 Ω, the impact of BTI on the measured current becomes more apparent. With the resistor combination of R_{G_TOP}/R_{G_BOT} = 33 Ω/220 Ω, the impact of BTI on the shoot-through current, through V_{TH} becomes clear. In conclusion, it is recommended to use a combination that exaggerates the shoot-through charge so that subtle changes in V_{TH} can be more easily detected.

The device itself plays also a fundamental role in the effectivity and applicability of this methodology, as the results presented from Fig. 2 to Fig. 5 indicate. In order to evaluate the impact of the gate stress on the different devices, they were subjected to accelerated gate stress tests and the impact on the shoot-through current was characterized. Fig. 7(a) shows the measured shoot-through current for a SiC trench MOSFET from ROHM, unstressed and after cumulative one hour stresses of V_{GS}=-35 and V_{GS}=-38 V at 150 °C whereas Fig. 4(b) shows the measured shoot-through current for a SiC planar MOSFET from Cree/Wolfspeed, unstressed and after cumulative one hour stresses of V_{GS}=-25 and V_{GS}=-30 V at 150 °C. For both devices, the gate resistances used were R_{G_TOP} = 33 Ω/R_{G_BOT} = 220 Ω and the characterization was done after 16 hours relaxation at V_{GS}=0.

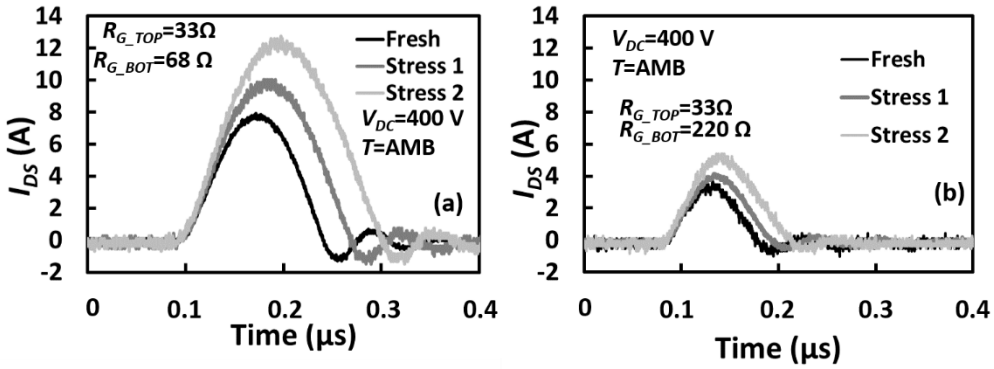

Fig. 7 Impact of highly accelerated NBTI stresses on the shoot-through current (a) SiC Trench from ROHM (b) SiC Planar from Cree/Wolfspeed

From the results above, it is clear that the shift of V_{TH} affects the shoot-through current, with more apparent results for the evaluated trench MOSFET. This indicates that the shoot-through current and charge can be suitable cursors of BTI-induced V_{TH} shifts.

Test method for evaluation of V_{TH} shifts using cross-talk

In the tests presented previously the results depend on the gate voltage selected for the accelerated stress tests and the resulting V_{TH} shift. The impact of the peak shift of V_{TH} after stress and subsequent recovery [19] are not captured, which would be paramount for assessing the impact of BTI-induced V_{TH} shifts. Hence, the test methodology shown in Fig. 8 is proposed, which allows to capture the impact of the peak shift and recovery using the shoot-through current.

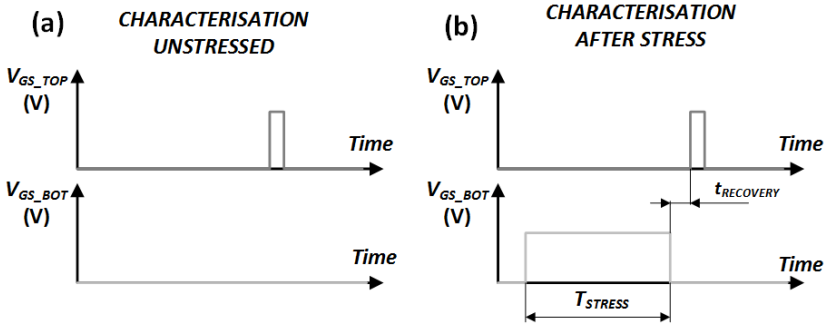

Fig. 8. PBTI stress and characterization pulse sequence (a) No stress (b) PBTI stress and recovery

As shown in Fig. 8(a), similar to the characterization performed in the previous sections, a gate pulse is applied to the top device turning it ON while the bottom device is held OFF at V_{GS} = 0. This is used to characterize the shoot-through current of the unstressed (fresh) device. To evaluate the impact of the stress and recovery, the test sequence shown in Fig 8(b) is used, which in this figure is shown for the PBTI stress sequence.

A gate pulse of duration T_{STRESS} is applied to the bottom device and depending on the value of V_{GS_BOT} and T_{STRESS}, the shift of V_{TH} will be higher or lower. After the stress is removed, the characterization pulse is applied after a determined recovery time $t_{RECOVERY}$, while holding V_{GS_BOT} at 0 V. This allows to evaluate the impact of V_{TH} shift and the subsequent recovery can be evaluated if the value of $t_{RECOVERY}$ is increased. Similar pulses can be applied for NBTI, but using a negative stress voltage. A modified gate driver is required to allow gate voltages of 0 V and $-V_{GS\_BOT}$.

Using the proposed methodology, the impact of the recovery time on the shoot-through current can be characterized, measuring the shoot-through current after different $t_{RECOVERY}$ values. As the power dissipated during the test is high, due to the simultaneous occurrence of high voltage and high current, the stress and characterization sequence has been applied for each measurement point, allowing a long recovery time (180 s) between measurements. The objective of this is to avoid the self-heating of the device, as V_{TH} is also temperature dependent. An aluminum heater/heatsink was attached to the device and the temperature was monitored, resulting in a negligible temperature increase for single event shoot-through currents. For characterizing the non-stressed DUT, the shoot-through current is measured without applying any stress to the bottom device, holding the gate at 0 V.

The method proposed in this paper has been evaluated for both positive and negative stresses using the devices with a higher shoot-through current, hence the impact of BTI-induced threshold shifts will be more apparent and easier to identify. The devices are the SiC trench MOSFET from ROHM and the SiC planar MOSFET from ST. The stress and characterization measurements were performed at ambient temperature, using a stress of 20 V and 10 s duration for the evaluation of PBTI and a stress of -26 V and 10 s duration for the evaluation of NBTI.

The results for PBTI evaluation of the SiC planar MOSFET from ST are shown in Fig. 9, where Fig. 9(a) shows the measured shoot-through current transients, Fig. 9(b) shows the peak shoot-through current as a function of the recovery time and Fig. 9(c) shows the shoot-through charge as function of the recovery time. The gate resistors combination was R_{G_TOP}=33Ω/R_{G_BOT} =220Ω and the DC link voltage was 400 V.

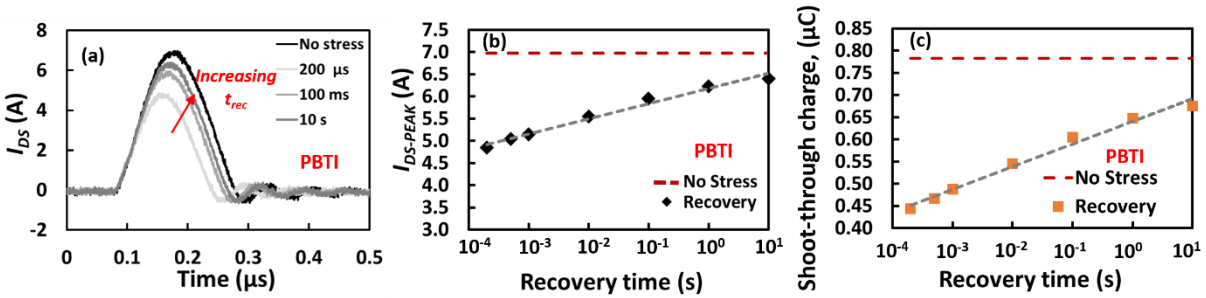

Fig. 9 Impact of PBTI stress (+20 V/10 s at ambient temperature) - SiC planar MOSFET ST (a) Shoot-through current transients, (b) Peak shoot-through current as function of the recovery time, (c) Shoot-through charge as function of the recovery time

As shown in Fig. 9, the positive gate voltage stress results in a positive shift of V_{TH} that causes a reduction of the shoot-through current (light grey). As the recovery time increases after stress removal and V_{TH} reduces to its pre-stress value, the shoot-through current increases to its pre-stress value (black). This is clearly observed in Fig. 9(b) and Fig. 9(c), analyzing the peak shoot-through current and charge.

The results for NBTI evaluation of the SiC planar MOSFET from ST are shown in Fig. 10, where Fig. 10(a) shows the measured shoot-through current transients, Fig. 10(b) shows the peak shoot-through current as a function of the recovery time and Fig. 10(c) shows the shoot-through charge as function of the recovery time. The gate resistors combination was R_{G_TOP}=33Ω/R_{G_BOT} =220Ω and the DC link voltage was 400 V.

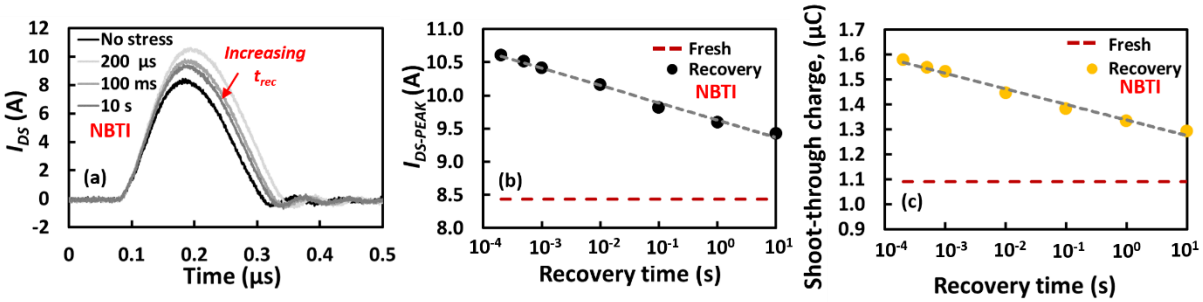

Fig. 10 Impact of NBTI stress (-26 V/10 s at ambient temperature) - SiC planar MOSFET ST (a) Shoot-through current transients, (b) Peak shoot-through current as function of the recovery time, (c) Shoot-through charge as function of the recovery time

In the case of the negative gate stress, as shown in Fig. 10, a negative shift of V_{TH} causes an increase of the shoot-through current (light grey), which reduces to its pre-stress value (black) as the recovery time increases, meaning an increase of V_{TH} with time after stress removal. The significance of these results is that they show the implications of the V_{TH} shift in a converter leg.

The difference in the shoot-through current transients in Fig. 9 and Fig. 10 can be attributed to the different gate driver circuit used for stressing the gate with a positive and a negative gate voltage. Analyzing the shoot-through charge and normalizing the values respect to the unstressed value in Fig. 9 and Fig. 10, for the ST SiC planar MOSFET and the positive gate stress the shoot-through charge reduced to 56.7% measured 200 µs after stress removal, recovering to 86.3% 10 s after the stress. In the case of the negative stress, stress the shoot-through charge increases a 44.8% measured 200 µs after the stress, recovering to an increase of 18.6 % 10 s after the stress.

Similar tests were performed with the SiC trench MOSFET from ROHM, but in this case the gate resistors combination was R_{G_TOP} = 33 Ω/R_{G_BOT} = 68 Ω. The results of the characterization tests are shown in Fig. 11 for PBTI evaluation and Fig. 12 for NBTI evaluation. The stress values were the same that the planar device, namely 20 V and 10 s duration stress for PBTI and -26 V and 10 s duration stress for NBTI.

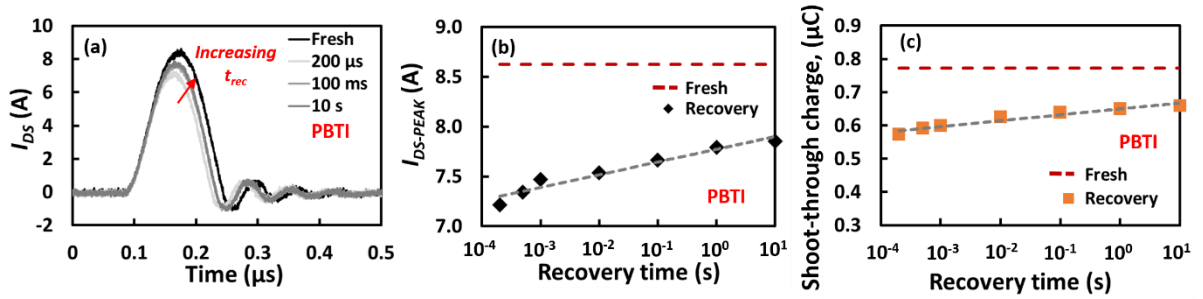

Fig. 11 Impact of PBTI stress (+20 V/10 s at ambient temperature) - SiC trench MOSFET ROHM (a) Shoot-through current transients, (b) Peak shoot-through current as function of the recovery time, (c) Shoot-through charge as function of the recovery time

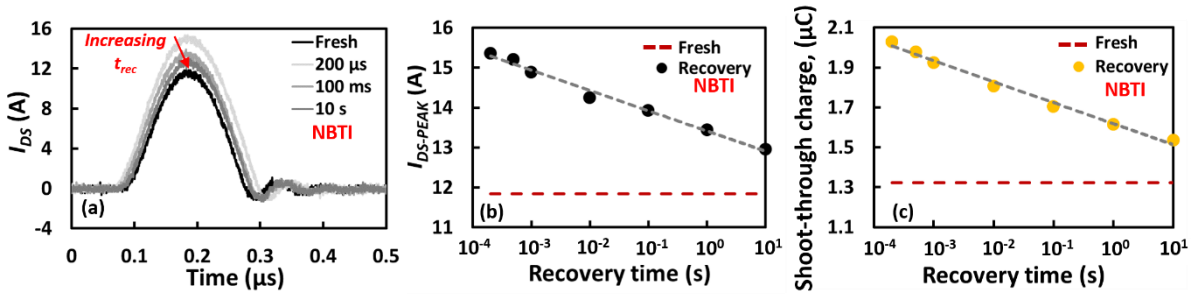

Fig. 12 Impact of NBTI stress (-26 V/10 s at ambient temperature) - SiC trench MOSFET ROHM (a) Shoot-through current transients, (b) Peak shoot-through current as function of the recovery time, (c) Shoot-through charge as function of the recovery time

For the ROHM SiC trench MOSFET, analyzing the shoot-through charge and normalizing the values respect to the unstressed value in Fig. 11 and Fig. 12, for the positive gate stress the shoot-through charge reduced to 74.2% measured 200 µs after the stress, recovering to 85.4% 10 s after the stress. In the case of the negative stress, stress the shoot-through charge increases a 53.5% measured 200 µs after the stress, recovering to an increase of 16.2% 10 s after the stress.

The method presented here could be used to evaluate the impact of temperature, stress duration and stress level, together with the impact of the recovery time on BTI-induced threshold voltage shifts in SiC MOSFETs.

Conclusion

In this paper a novel methodology for the evaluating the impact of BTI-induced threshold voltage shift on a leg converter operation has been presented. The method is based on the Miller coupling between two devices in the same phase and uses the shoot-through current from parasitic turn-ON to monitor V_{TH} and its impact. It has been shown how for NBTI evaluation, the negative gate stress causes a negative shift of V_{TH} which causes an increase of the shoot-through current and charge, with recovers (decreases) with time after stress removal. For PBTI evaluation, the positive gate stress results in a positive shift of V_{TH} resulting in a reduction of the shoot-through current and charge, with recovers (increases) with time after stress removal. The effectivity is dependent on the gate resistors combination used, as it requires a higher shoot-through current to make the impact of BTI-induced shifts more apparent. This method will be of interest of application engineers, as it can be used to evaluate the impact of BTI in a converter environment.

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